Subproject B3.6

Coherent Charge Manipulation using Arrays of Nano-Junctions

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1. Introduction and Summary

The project B3.6 is focused on experimental investigation of collective charge excitation in arrays of small capacitance Josephson junctions (SCJJs), namely Cooper pair solitons [1]. These charge excitations are predicted to be dual objects to magnetic flux solitons associated with supercurrent vortices in long Josephson junctions. Both types of solitons can be described by the sine-Gordon model, since both the array of SCJJs and the long Josephson junction can be viewed as transmission lines with nonlinearities derived from the Josephson equations. While flux solitons carry one magnetic flux quantum Φ_0, the charge solitons carry exactly the charge $2e$ of a Cooper pair distributed over several superconducting islands.

As rewarding practical aim, coherent control of the charge solitons should open the possibility to develop a quantum mechanically precise standard of electrical current. The quantum metrology of the current can be implemented by frequency locking of the charge propagation through an array of SCJJs. This locking at frequency f should yield voltage-independent plateaus at discrete current values $I = n \cdot 2e \cdot f$ of the current-voltage characteristics. Such frequency to current conversion would allow closing the remaining open side of the quantum metrological triangle [2,3], which connects frequency, voltage and current by quantum mechanical effects thus containing only fundamental constants. Previous attempts to close this side of the triangle failed due to the difficulties of providing the necessary current precision for metrological applications. The approach usually quoted [4] in this context derives from the single electron transistor (SET), which consists of a gated island connected to two leads via tunnel contacts. Since in normal metallic SET devices the charge carrier is localized on only very small islands, it is quite susceptible to background charge fluctuations and charges trapped in the substrate. In our case, the advantage of using Cooper pair charge solitons is that they extend over several islands and therefore their sensitivity to charge noise is expected to be significantly reduced.

The project was started in July 2009. During the past 18 months of this project, using CFN funds we have been mainly working on establishing fabrication of Josephson junction arrays using CFN facilities at KIT South Campus. At the same time, we set up at KIT South Campus low temperature measurements of externally produced arrays. At KIT South Campus we also did a theoretical work that will help our understanding of the charge soliton motion in the presence of disorder. The work was going on in close collaboration with the part of our group of KIT North Campus, were similar arrays were fabricated and measured in a dilution refrigerator. These measurements are presented in this report.

2. Experimental conditions

For studying charge solitons, it is very convenient to replace single Josephson junctions of the array by small superconducting loops with two Josephson junctions forming dc SQUIDs. This way, the Josephson coupling energy between the islands can be controlled by applying an external magnetic field perpendicular to the plane of the array. Each island has a capacitance C to each of its nearest neighbors and a capacitance to ground C_0. The conventional way of biasing the array requires applying the voltage difference between the two ends of the array. The screening length of the electrical field in the array coincides with the size of the charge solitons given by the characteristic

length $\Lambda = \sqrt{C/C_0}$, which is typically on the order of ten arrays cells. This length also describes the voltage distribution inside the array, meaning that the bias voltage drops exponentially near the ends of the array.

In order to observe and manipulate distinct charge solitons the array needs to be considerably longer than the soliton size Λ. We aim at fabricating arrays that are about 20 - 40 Λ long (meaning 200 - 400 islands). As the bias voltage quickly drops to zero near the ends of the arrays, the conventional biasing scheme gives basically no control over the charges deep inside the array. In order to solve this problem, we have suggested and are currently implementing a new design with uniformly distributed gate electrodes along the array. The capacitances between islands, array and ground can be chosen appropriately here in order to achieve a suitable Λ_g. The idea of this design is shown in Fig.1.This biasing scheme should result in a uniform bias voltage distribution along the array and thus to nearly constant electrical field acting on the charge solitons inside the array.

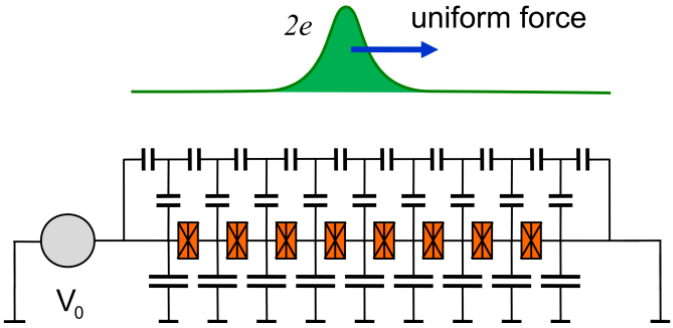

Figure 1: Principle of our uniform bias voltage approach. A chain of large capacitors distributes the voltage drop along the array. The electrodes of the capacitor "comb" are themselves weakly coupled capacitively to the arrays islands.

3. Fabrication of Josephson junction arrays

For the fabrication of Josephson junction arrays we deploy the suspended resist shadow evaporation technique [5], which we adapted for the fabrication of long arrays of Josephson junction cells. Shadow evaporation makes use of two resist layers of different sensitivity. This way, the top layer defines the shape of the structures, while the bottom layer is removed in a wider area during development. By choosing the appropriate angle between surface normal and evaporation source, one can change the position of the material deposited under the suspended resist pattern. To produce tunnel junction with this technique, free-hanging parts of the top resist are required. These resist elements are called Dolan bridges.

We selected an electron beam resist stack system suited for the shadow evaporation of aluminum. The electron beam parameters and the development process were optimized in order to get maximum possible resolution as well as stable Dolan bridges with sufficiently large undercut. A vacuum chamber equipped for thermal evaporation of thin aluminum films was set up in KIT Campus South lab and adapted for precise control of oxidation parameters.

In order to provide electrically contact the arrays, bonding pads and leads had to be pre-processed silicon chips. We have chosen for the contact pads an alloy of gold and palladium, which offers the advantages of unoxidized, high impedance noble metal contacts. Pure gold tends to alloy high

ohmically with aluminum, and forms islands instead of films up to a critical thickness, while pure palladium is known to catalyze unwanted chemical reactions in the resist. The alloy also has a high electron beam microscopy contrast against the silicon chip and the e-beam resists, which is essential for aligning the shadow evaporation layers to the leads.

The designed Au/Pd pads layout has leads that are impedance matched for coupling microwave signals to and from the array. It also provides a large number of DC contacts to the arrays. We optimized the design for maximum alignment precision. For the fabrication of this layer, we use instead of electron beam the much faster optical lithography. We have also acquired the equipment necessary to make photo-masks in order to parallel process Au/Pd leads onto several chips at once. The masks are written with the direct writing laser (DWL 66) in CFN clean room.

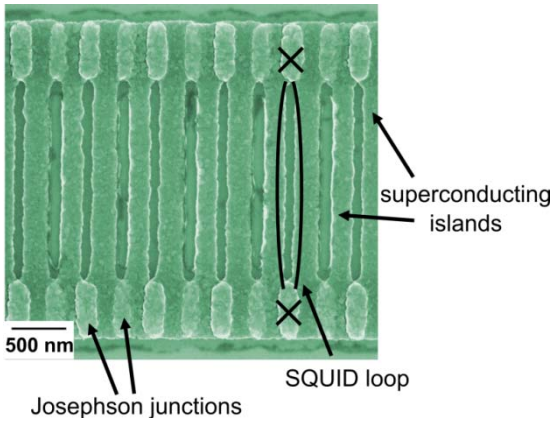

Figure 2: SEM micrograph of a section of an Al-based Josephson junction array fabricated at CFN. The use of SQUIDs gives us control over the effective Josephson energy via applied magnetic field.

Placing the uniform voltage bias electrodes near the arrays during the lithography step defining the arrays themselves proves to be rather difficult. The beam electrons are back scattered by the substrate and influence the resist nearby, thus locally modifying the optimal resist exposure dose. We chose to circumvent this problem and avoid this proximity effect [6] by structuring the uniform bias electrodes in a third lithography step (an example of such structure is shown in Fig. 3).

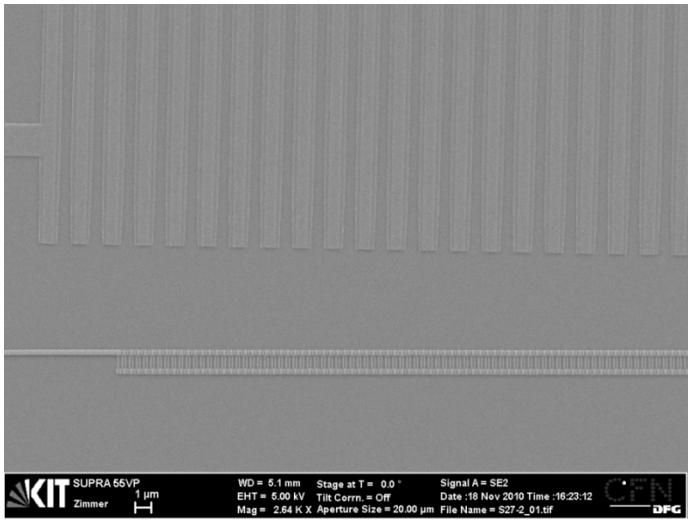

Fig. 3: SEM micrograph of an array with bias gates electrodes, fabricated in three lithography steps.

4. Experiments

There are two characteristic energies that determine the properties of the Josephson junction arrays: the charging energy E_C and the Josephson energy E_J. In order to see charging effects, E_C must be at least comparable to E_J. Both energies need to be much bigger than the thermal energy k_BT. In our circuits, we tuned the ratio E_J/E_C by applying the magnetic field perpendicular to the sample plane.

We employed two different experimental setups to measure Josephson junction arrays at mK temperatures: one that was already in place at KIT North Campus and another at KIT South Campus which we adapted for high-ohmic picoampere measurements in the course of this project.

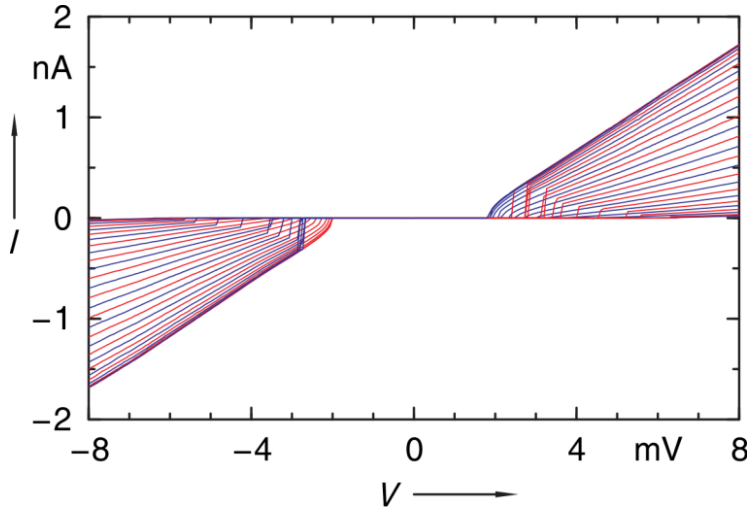

Figure 4: *IV*-curves of an array fabricated and measured at KIT North Campus. It had 255 junctions, and the zero-field ratio of $E_J/E_C \sim 1$. Voltage was swept back (blue) and forth (red), and the coupling energy E_J was reduced via external magnetic field (lower curves have lower energy). Around zero voltage, the coulomb blockade is clearly visible. The conductance in the resistive slope scales proportional to E_J^2.

The measurements performed at KIT North Campus were focused mainly on DC properties of arrays that were also fabricated at CN. A typical measurement consisting of a sequence of current-voltage (*IV*) curves, as shown in Fig.4. The bias voltage here was applied conventionally between the ends of the array and swept forth and back. Changing the external magnetic field results in a different Josephson coupling energy E_J between the islands. Figure 4 represents a typical *IV*-characteristic of an array of comparably small Josephson energy ($E_J/E_C \sim 1$ at zero magnetic field and less for non-zero field). The array clearly exhibits the Coulomb blockade at low bias voltages. The array switches to non-zero current state at some critical voltage depending on E_J. On the sweep back, the array *IV*-curve displays a hysteresis. Our key finding here is that the conductance of the hysteretic arrays in the charging regime scales proportionally to E_J^2 [B3.6:1]. The resistive slope can be interpreted via the so-called *P(I)* theory as incoherent Cooper pair tunneling.

The second measurement setup at KIT South Campus was in the course of this project newly adapted for the high precision measurement of picoampere currents. We implemented and tested the effect of microwave irradiation to the sample *IV*-characteristics. Figure 5 shows *IV*-curves taken at this setup. We used a sample provided by the group of D. Haviland of KTH Stockholm. The array had the zero-field ratio of $E_J/E_C \sim 4$. The plot shows the transition from a nearly superconducting state (upper curves) to a state with a pronounced coulomb blockade, if only for voltages up to several 100 μV (superconductor/insulator phase transition).

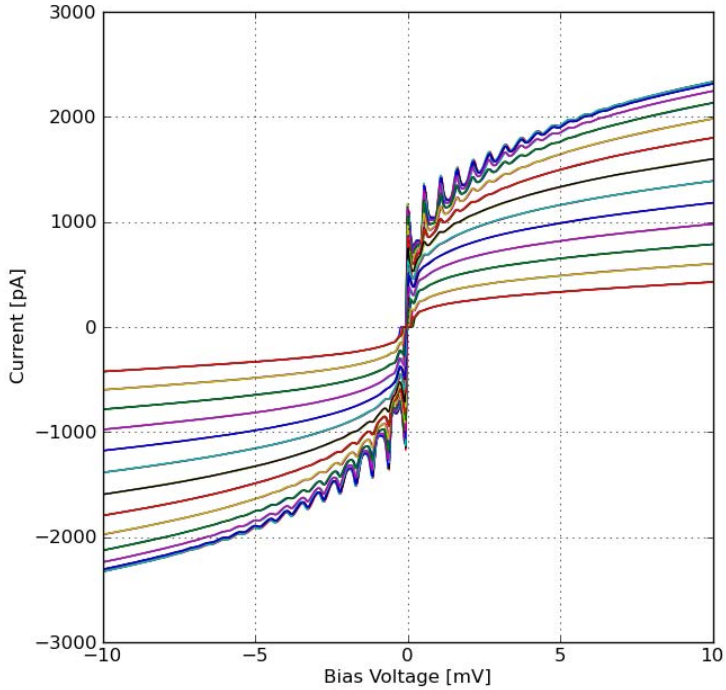

Figure 5: *IV*-curves of the array provided by D. Haviland (KTH Stockholm), measured in the setup at KIT South Campus. The array had 384 SQUIDs with zero-field ratio of $E_J/E_C \sim 4$. Lower curves (close to zero current level) have lower Josephson energy. Around the smallest E_J values the array exhibits a superconductor/insulator transition.

Besides studying arrays of small Josephson junctions, we investigated experimentally and theoretically the behavior of small junctions under microwave irradiation [B3.6:2]. This study appears rather relevant for better understanding of junction arrays. The measured low-voltage resistive states display strongly smeared incoherent Shapiro-like steps in the current–voltage characteristics. This behavior appears when both thermal fluctuations and high frequency dissipation are strong. A theoretical analysis based on incoherent multi-photon absorption by a junction biased in the Josephson phase diffusion regime is in good agreement with the experimental observations [B3.6:2]. Here we can argue that the microwave-assisted incoherent tunneling processes should have their counterpart in the dual charge regime, and thus become relevant for propagation of charge solitons through the array associated with incoherent Cooper pair tunneling [B3.6:1].

5. Theoretical work

In connection with our experiments on charge solitons in arrays, we performed a series of numerical simulations in discrete sine-Gordon model with spatial disorder associated to background charges randomly placed on the substrate [B3.6:3]. This static charge disorder leads to pinning of solitons and thus hinders their motion. We studied the maximum pinning force depending on the soliton size Λ measured in units of array cells. We find that random charges are most effective for the case of large discreteness ($\Lambda \sim 1$) and modify the conventional Pierls-Nabarro barrier. Good news here are that disorder effects become irrelevant for large soliton size of $\Lambda > 5$ or more array cells. Once the Cooper pair soliton size becomes much larger than the variation length scale of random charges

(from cell to cell) the soliton hardly notice any pinning. The results of this simulation and their comparison with theory are presented in Fig. 7.

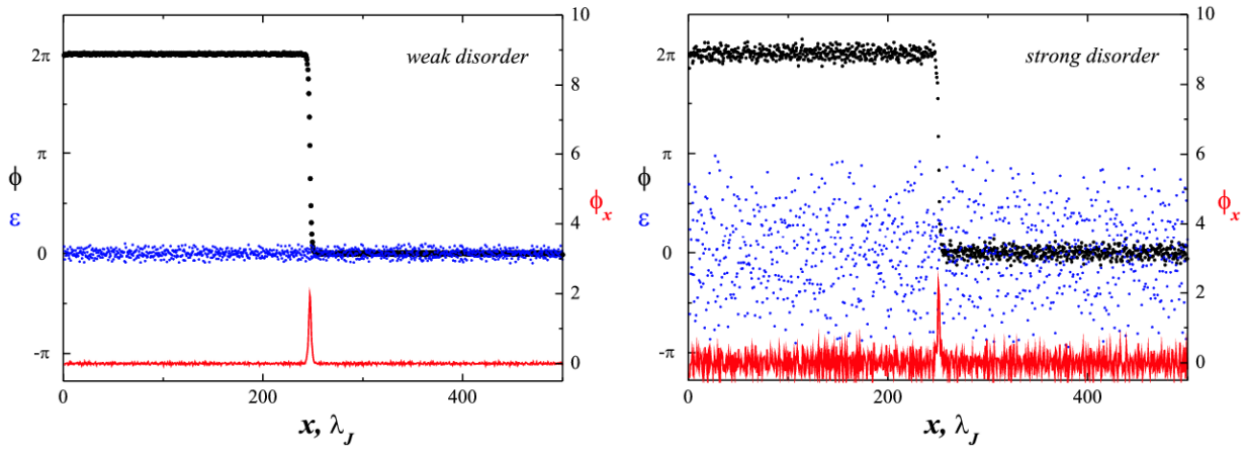

Figure 6: Numerical simulations [B3.6:3]. A charge soliton (red line) in the presence of random offset charges on the array islands (blue dots).

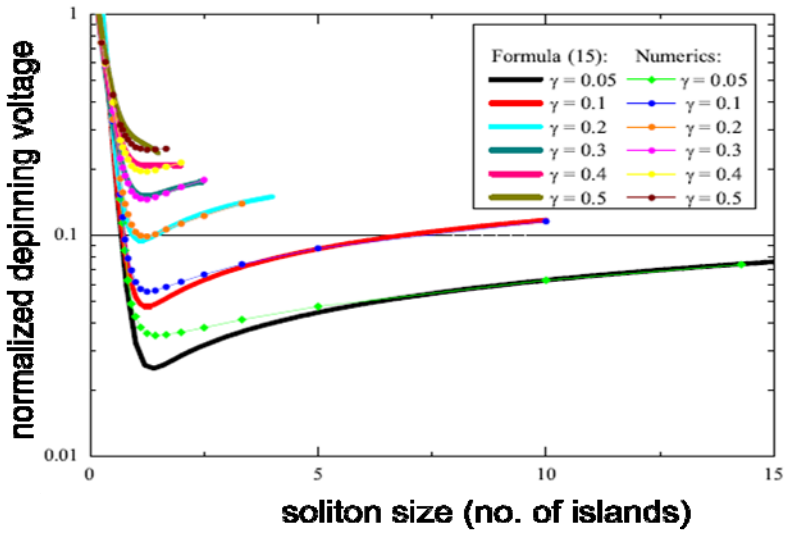

Figure 7: Soliton pinning on background charges versus the soliton size [B3.6:3]. Numerical simulation data (dots) are compared with the analysis (lines).

6. Service for other CFN Projects

The performed experimental and numerical work within B3.6 was done in close interaction with the theoretical subproject B3.7 led by Alexander Shnirman. In particular, the study of "compact" charge solitons reported in Ref.[7] is motivated and directly related to experiments performed here. We suppose that the conductance scaling proportional to $\sim E_J^2$ [B3.6:1] can be explained in terms of the effective soliton mass derived by Shnirman and co-authors [8].

7. References

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